

FIG. 1
(Prior Art)

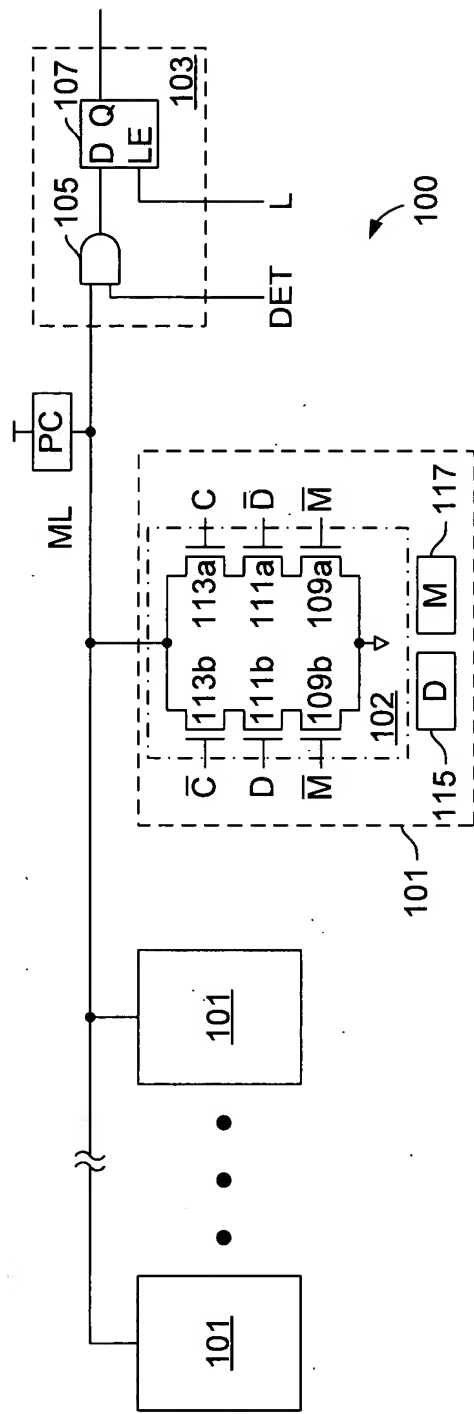
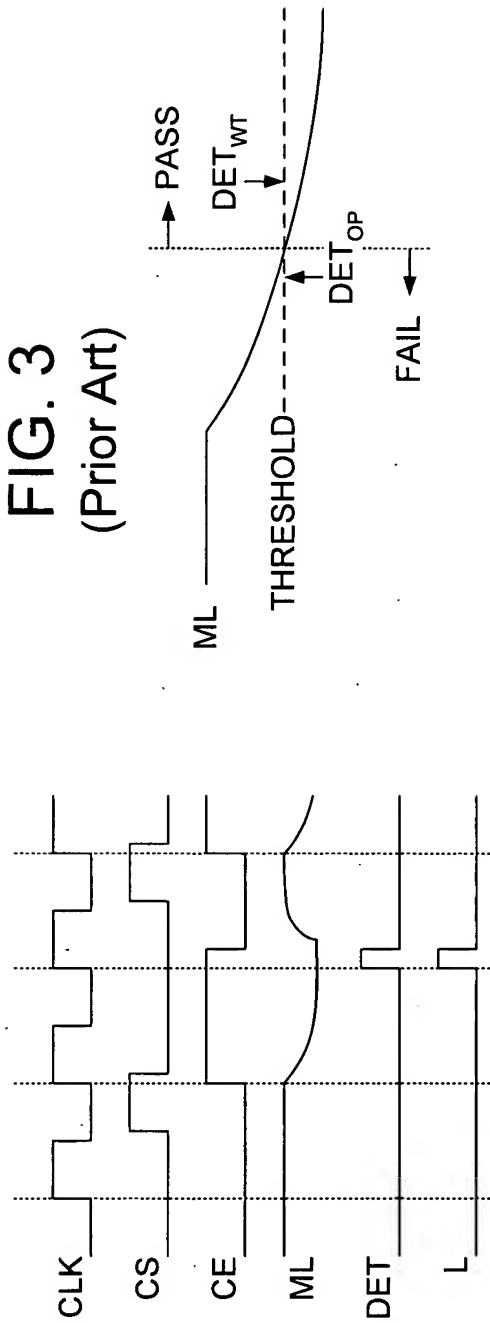


FIG. 3
(Prior Art)



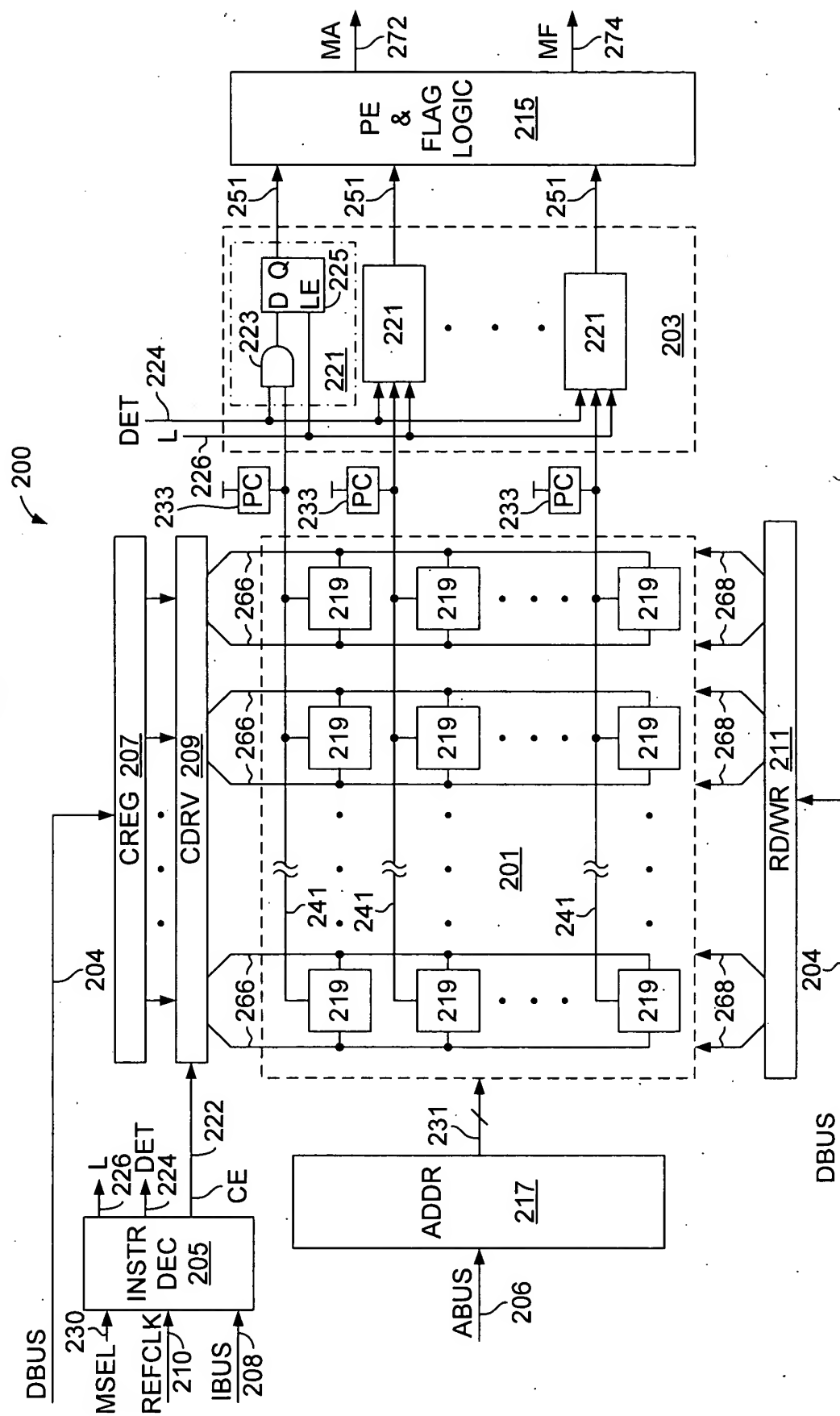
[illegible]

FIG. 5 is a block diagram of a data path 300. It includes an N-MODE TIMING GENERATOR 301 and a T-MODE TIMING GENERATOR 303. Both generators receive a common clock signal CLK 302 and a control signal CS 304. The N-MODE TIMING GENERATOR 301 outputs signals L_{NM} 308, DET_{NM} 306, and L 226. The T-MODE TIMING GENERATOR 303 outputs signals L_{TM} 312, DET_{TM} 310, and DET 224. These signals are fed into a multiplexer 310, which is controlled by MSEL 230. The multiplexer 310 has two data inputs (0 and 1) and one output 305.

FIG. 6 is a detailed circuit diagram of the data path 300. It shows the internal logic of the timing generators and the multiplexer. The N-MODE TIMING GENERATOR 301 consists of a D flip-flop 361, a D flip-flop 363, and an output stage 365. The T-MODE TIMING GENERATOR 303 consists of a D flip-flop 371, a delay block DLY 373, and an output stage 375. The multiplexer 310 is implemented with two 2-to-1 multiplexers 381 and 383, and an output stage 355. The circuit is controlled by DCTL 372 and MSEL 230. The output of the multiplexer 310 is 305.

FIG. 6

FIG. 7

